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A novel phase-coherent programmable clock for high-precision arbitrary waveform generation applied to digital ion trap mass spectrometry

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ABSTRACT

Digital ion trap (DIT) mass spectrometry requires the ability to precisely and accurately produce waveforms. The quality of the mass spectra produced in terms of resolution and mass accuracy depend on the resolution and precision of the applied waveforms. This publication reveals a novel method for the production of arbitrary waveforms in general and then applies the method to the production of DIT waveforms. Arbitrary waveforms can be created by varying the clock frequency input to a programmable read only memory that is then input to a digital-to-analog converter (DAC). The arbitrary waveform is composed of a defined number of points that are triggered to be written after programmed numbers of clock cycles to define the arbitrary waveform. The novelty introduced here is that the direct digital synthesis (DDS) generated clock frequency can be precisely changed as the arbitrary waveform is written because we have developed a method to rapidly switch the DDS frequency exactly at the end of the output clock cycle allowing exact timing of multiple transitions to produce precise and temporally complex waveforms. Changing the frequency only at the end of the output clock cycle is a phase-coherent process that permits precise timing between each point in the arbitrary waveform. This waveform generation technique was demonstrated by creating a prototype that was used to operate a digital ion trap mass spectrometer. The jitter in the phase-coherent DDS TTL output that was used as the frequency-variable clock was 20 ps. This jitter represents the realizable limit of precision for waveform generation. The rectangular waveforms used to operate the mass spectrometer were created with counters that increased the arbitrary jitter to 100 ps. The mass resolution achieved was 5000 at $m/z = 414$. Resolution should improve with increasing mass because the waveforms have longer periods while the jitter should remain constant. Given the current limit of the variable clock resolution, much better mass resolution should be achievable with future generations of the waveform production system. The agility of the DDS function generators permits the phase-coherent variable clock to be switched at a rate up to 250 MHz. This permits arbitrary waveforms to be produced with much more temporal complexity than previously possible.

1. Introduction

Digital ion trap (DIT) mass spectrometry has been developed in the last decade [1–3]. It has enormous potential for the analysis of large molecules and particulate ions because its mass range is essentially limited only by the ability to trap ions. Currently, inroads are being made in trapping particulate ions sampled from the atmosphere [4–6]. As these technologies come into use, the utility of DITs will increase.

One of the biggest problems in producing a DIT is the production and control of the digital waveforms. In general, DITs operate by scanning or stepping the frequency of the trapping and/or excitation waveforms. These frequencies must be changed rapidly to produce a mass scan. The correlation between the ejected mass and the waveform frequency is not a linear function [7]. Consequently, the waveforms must be scanned or stepped nonlinearly for the ejection mass to correlate linearly with time during a scan. DITs operate with rectangular waveforms. The stability region of the ions in the trap varies with the duty cycle of the trapping waveform [8]. Changing the duty cycle provides a quick method of mass selection. Modifying the duty cycle of the trapping waveform is equivalent to adding a DC component to the trapping field [8,9]. If a digitally operated linear quadrupole is used as a mass filter, the duty cycle sets the width of the mass window for the transmitted ions. Additionally, the duty cycle of the excitation waveform can be varied and its phase can be adjusted to optimize resolution [3]. Precise control of the waveforms in terms of frequency, amplitude, phase and duty cycle is extremely

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important to the practice of digital ion trap mass spectrometry.

When we started this project, a commercially available method for producing and changing the rectangular waveforms needed for DIT mass spectrometry did not exist. Ding et al. [3] produced the waveforms for their DIT using direct digital synthesis (DDS). They used a field programmable gate array (FPGA) to rapidly change the frequency of the waveforms and scan the mass spectrum. They also accomplished pulse width modulation of the excitation waveform (changing the duty cycle) with 8-bit control (1 part in 256). Pulse width modulation using DDS can be accomplished with an external DAC to set the level of the comparator used to create the rectangular waveform from the filtered sine output. Theoretically, duty cycle modulation can be accomplished with up to 16-bit control (1 part in 65,536) based on the resolution of the DAC used to control the comparator. Ideally, better precision and accuracy in producing the rectangular waveforms will yield better resolution and accuracy in digital ion trap mass spectrometry.

With this information, we set about creating an agile waveform generator. We decided to use DDS technology as the basis for our waveform generator because the frequency can be changed as fast as the phase word can be downloaded to the device and the waveforms can be generated with up to 48-bit frequency resolution. Upon reviewing the methodologies used to generate waveforms, we further decided that the best course was to use the DDS to create a frequency-variable clock that could be used to read out arbitrary waveforms.

The idea of writing an arbitrary waveform into programmable memory and then using a frequency-variable clock to read the waveform into a digital-to-analog converter (DAC) to create arbitrary waveforms is old. It is schematically depicted in Fig. 1. In the earliest versions, all of the waveform points within the memory were played out on each cycle and the frequency of the arbitrary waveform was defined by the frequency of the clock, $F_{arb} = F_{clock}/N$, where N is the number of points that define the arbitrary waveform. Memory segmentation and sequencing were rapidly developed to create more complex arbitrary waveforms requiring smaller amounts of memory. In these strategies, the variable clock defines all of the temporal characteristics of the arbitrary waveform.

Currently, many arbitrary waveform/function generators use DDS technology to create arbitrary waveforms and other functions. This technology uses an internal clock, a phase accumulator, memory for waveform storage or a look-up table, a DAC and a low-pass filter [10]. The greatest advantage of this technology is that it can provide frequency resolution to millihertz levels [11]. The disadvantages are waveform jitter and the lack of sequencing capability. Waveform jitter results from up or down sampling of the waveform when the frequencies are not equal to the clock frequency divided by the waveform length or submultiples. This results in missing samples and temporal jitter [10]. This disadvantage could be circumvented if the DDS-based waveform generator could be operated with an external variable clock; however an external signal cannot be used to clock out the waveform in typical commercial DDS waveform generators [12]. The inability to segment the memory and piece the segments together (sequencing) to create large waveforms without the use of massive amounts of memory also limits the complexity of the waveforms produced by direct digital synthesis.

More recently, waveform generators have been produced that permit the use of an external variable clock and permit sequencing to produce complex waveforms [12]. These generators can take advantage of the phenomenal frequency resolution of DDS by using it to generate the external clock signal. The limitation of this technique is that frequency of the clock cannot be changed during the production of the waveform. That is, the spacing of the points in the waveform cannot be changed once the clock frequency is set. DDS technology permits precise definition of the timing in the waveform provided that all of the required transitions in the waveform occur at integer increments of the DDS clock waveform period. If not, then the DDS clock frequency has to rapidly change during the creation of the waveform and the change has to occur consistently and predictably. Unfortunately, that is not possible with the current state of DDS technology.

Normal direct digital synthesis occurs as follows [10]. A 24–48-bit word defines the stepping of the phase of a sine wave in a phase accumulator. The phase is accumulated at a fixed frequency defined by a reference clock. The accumulated phase is referenced to a sine look-up table that defines the y-value of the sine as a function of phase. This y-value is then input to a DAC. The DAC steps through the y-values of the sine wave at a rate defined by the reference clock. The stepped sine wave from the DAC is then passed through a filter that removes the high frequency components to yield a smooth sine wave whose frequency and resolution is defined by the stepping of the phase rather than the reference clock frequency (see Fig. 2).

The frequency-switching process of the DDS can occur as fast as the word that defines the stepping of the phase can be downloaded to the DDS chip. This rate is defined by speed of the control interface and the loading configuration selected. Typically, DDS devices provide a parallel byte load to facilitate getting data into the control registers. Control data clocking rates of 100 MHz are generally supported for the byte load parallel control interface. This means that a new tuning word can be loaded to the DDS every 10 ns. Switching of the frequency can happen at any point in the phase accumulation and yield very different waveforms during the transition. To illustrate this point, we have plotted the accumulator, sine look-up and the comparator outputs from a DDS device for a factor-of-5 reduction in frequency that occurs at various points in the phase accumulation process in Fig. 3.

Consequently, the output waveforms during frequency stepping may be quite different. We call the fluctuations of the frequency

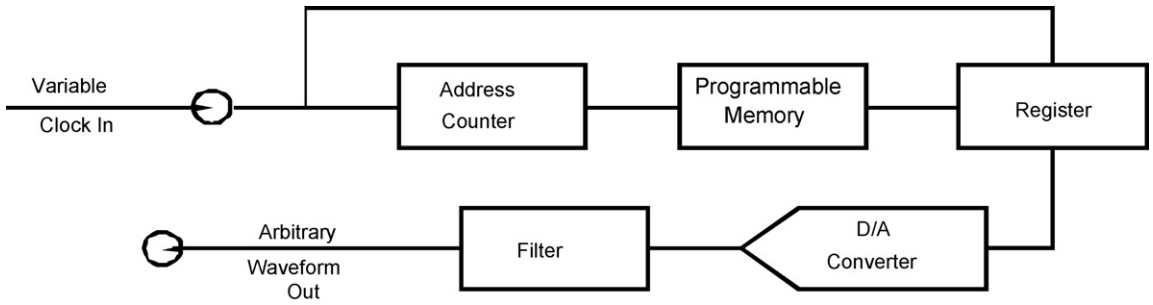

Fig. 1. A schematic depiction of arbitrary waveform generation with a variable clock. A waveform is written into memory. The frequency of a variable clock is then set to define the rate at which the points that define the amplitude of the waveform are read into a digital-to-analog converter to create the digital arbitrary waveform that is then passed through a low-pass filter to remove the high frequency components and create a smoothed arbitrary wave.

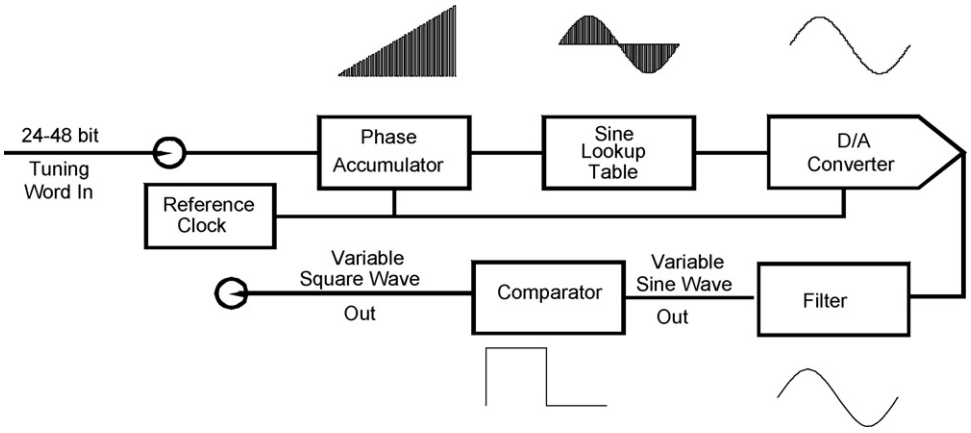

Fig. 2. A 24–48-bit word defines the stepping of the phase of a sine wave in a phase accumulator. The phase is accumulated at a fixed frequency defined by a reference clock. The accumulated phase is referenced to a sine look-up table that defines the y-value of the sine as a function of phase. This value is then input to a digital-to-analog converter (DAC). The DAC steps through the *y*-values of the sine wave at a rate defined by the reference clock. The digitally stepped sine waveform created by the DAC is then passed through a filter that removes the high frequency components to yield a smooth sine wave whose frequency and resolution are defined by the stepping of the phase rather than the reference clock frequency.

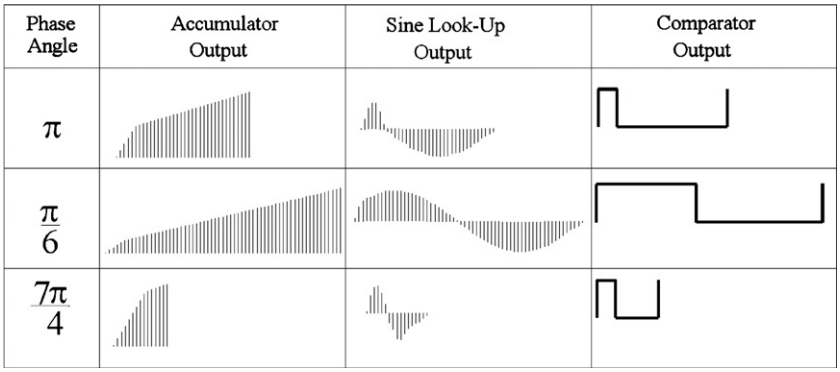

Fig. 3. In the DDS waveform synthesis process, changing the frequency occurs by changing the rate of phase accumulation. The frequency transition can happen at any value of the phase in the phase accumulation process to produce very different output waveforms during the transition. To illustrate this point, we have plotted the phase accumulator (left), sine look-up (center) and the comparator (right) outputs from a DDS device as a function of time for a factor-of-5 reduction in frequency that occurs at the phase angles on the left side of the chart. Each tier in the chart presents a different phase angle in the accumulation process for the frequency transition to occur. The length of each vertical line in the accumulator output represents a value of the phase angle (0–2π). The length of each vertical line in the sine look-up output represents the amplitude of the sine wave for each corresponding value of the phase from the accumulator. The change in the slope of the accumulator reveals when the frequency transition occurs. The spacing of each vertical line in the accumulator and sine look-up outputs is equal and represents the period of the internal DDS reference clock. This figure illustrates how varied the period of the wave can be during a frequency step in the normal DDS process.

transition, "DDS frequency transition jitter." The maximum temporal width of this jitter is equal to the difference in the periods of the two DDS frequencies. Those temporal differences can be substantial. For example, switching from 500 kHz to 1 MHz yields up to 1 μs frequency transition jitter.

Ideally, clock frequency changes could be used during the creation of an arbitrary waveform to change the spacing of the points that make up the wave. This could allow precise temporal definition of the transitions in the wave, thereby allowing the creation of much more complex and precise waves. The superb frequency resolution of the DDS could be used to precisely set the spacing of the points used to create the arbitrary wave. Unfortunately, the uncertainty in the temporal positions of the transitions caused by the DDS frequency transition jitter makes the waveforms produced by this process too jittery to be useful. Consequently, the best current commercial arbitrary waveform creation technology uses either a very high frequency fixed clock or a variable frequency clock to read out the arbitrary waveforms with a fixed temporal spacing between the points.

To eliminate timing errors during production, the arbitrary waveform features or transitions have to begin and end at the same phase of the clock waveform regardless of the clock frequency. We define this property as phase coherence. It is distinguished from the term "phase continuous" that is a feature of all DDS devices where the new frequency is programmed into the DDS and the next phase value in the accumulator is simply the last phase value of the waveform at the previous frequency incremented by the new phase word. In both cases, there is no phase discontinuity or glitch. However, with the normal DDS operation, if the frequency is switched to another value and then back again, the phase relationship will change every time a transition is made. With phase coherence, the frequency transition always occurs at the same phase value. This publication provides and demonstrates a new method for changing the DDS frequency phase coherently without any transition jitter. Our advance opens the possibility for precise timing of complex events. It enables the production of complex waveforms with unprecedented temporal precision and reproducibility.

A "glitched" sine wave is often used to compare the currently available commercial technology for producing arbitrary waveforms. Fig. 4(a) illustrates a "glitched" or notched sine wave from a DDS-based arbitrary waveform generator. The image depicts the jitter that results from sampling error that can occur when the arbitrary waveform period is not an integer multiple of the clock period. At higher repetition rates, the waveform can be under sampled causing the glitch to be missed. Fig. 4(b) illustrates a "glitched" sine wave from a variable clock-based arbitrary waveform gener-

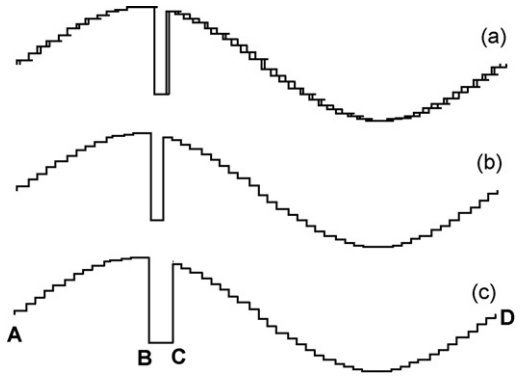

Fig. 4. (a) Illustration of a "glitched" sine wave from a DDS-based arbitrary waveform generator. The image depicts the jitter that results from sampling error. It occurs when the arbitrary waveform period is not an integer multiple of the clock period. At higher repetition rates, the waveform can be under sampled causing the glitch to be missed. (b) Illustrates a "glitched" sine wave from a variable clock-based arbitrary waveform generator. The clock rate can be set so that the arbitrary waveform period is an integer multiple of the clock period alleviating the sampling error issue. Here the transitions that create the glitch are defined at integer multiples of a single clock frequency (c) Illustrates a "glitched" sine wave generated using an agile, phase-coherent clock that permits the glitch to be located at any phase in the waveform with essentially any width. Here the frequency and interval sampling can be separately defined from point A to B, B to C and from C to D to precisely define the glitched sine wave without any sampling error and with a great deal more specificity.

ator that can change the clock rate so that the arbitrary waveform period is an integer multiple of the clock period thereby alleviating the sampling error issue. The transitions that create the glitch are defined at integer multiples of a single clock frequency. Fig. 4(c) illustrates a "glitched" sine wave generated using an agile phase-coherent clock that permits the glitch to be located at any phase in the waveform with essentially any width. The frequency and interval sampling can be separately defined from point A to B, B to C and from C to D to precisely define the glitched sine wave without any sampling error and with a great deal more specificity. The frequency of the arbitrary waveform can be changed by some factor by multiplying the clock frequency at each interval by the same factor. Our agile, phase-coherent, variable clock method for generating arbitrary waveforms permits very complex waveforms to be produced with great precision. The complexity of the waveform that can be produced depends on the number of intervals or transitions in the waveform. The frequency-switching rate is limited to 100 MHz with the 300 MHz, 48-bit DDS used in our prototype.

There are faster DDS waveform generators. A 1 GHz, 32-bit device would also yield a small temporal increment to the waveform period relative to the temporal jitter. At 10 MHz, a unit increase to the tuning word would yield approximately a 10^{-15} s change in the DDS-produced waveform period. The advertized frequency update rate for the parallel input version of these devices is 250 MHz with an analog output frequency up to 400 MHz. This agility permits arbitrary waveforms to be produced with much more temporal complexity than ever before. Once achieved, we predict that the impact of this development will be subtle yet it could be transformational because this achievement provides a second variable to the creation of arbitrary waveforms.

For the application to digital ion trap mass spectrometry, this frequency-switching method provides a highly resolved and precise way of setting and changing the duty cycle during a scan. Precise control of the duty cycle in digital quadrupole mass spectrometry is important. Changing the duty cycle is equivalent to adding a DC component to the quadrupole field [8,9]. It can be used for precise ion isolation in an ion trap or exactly setting the ion transmission window in a digitally operated quadrupole mass filter. Phase-coherent frequency switching makes precise arbitrary digital waveform production possible. This publication presents and demonstrates the frequency-switching method that makes this possible.

2. Precise triggering of DDS frequency transitions

DDS frequency transitions can be made to occur only at the end of the period of the DDS waveform by using two DDS chips operating with the same reference clock and the same phase increment word. The two DDS chips have to be phase shifted with respect to each other so that the output of the first is ahead of the other by an integer number of phase points, n. The output of the first DDS is converted to a square wave with a comparator. The trigger to change frequency of both chips is synchronized to the square wave output of the first DDS chip. The rising edge of the square wave correlates with the positive transition of the filtered sine wave through zero of the first DDS output. It also correlates with the roll over of the accumulator through zero (if the phase accumulation process was continuous and not stepped). The phase difference of the DDS chips can be set so the rising edge of the square wave output of the first DDS coincides with the last sampling point of the second DDS before its accumulator rolls over. By synchronizing the frequency transition of both DDS with the leading edge of the square wave of the first DDS, the stepping of the accumulator (frequency tuning word) can change when the accumulator passes through zero for the second DDS. Note that the phase accumulators in each DDS chip must be reset at each frequency transition in order to maintain the prescribed phase relationship between the two DDS. The triggering of the frequency switch will occur on the picosecond time scale, while the stepping of the accumulator happens on the nanosecond time scale. This innovation is predicated on the ability to calculate and keep track of the phase shifts for each cycle of the output and then adjust the phase shifts for each frequency transition so that the cycles begin and end when the phase of the sine is zero. These calculations and adjustments are calculated and loaded into first-in-first-out (FIFO) memory prior to running the scan.

The phase shifts are easily and precisely calculated by first determining the number of remaining points in the phase accumulator after N cycles of the DDS output just before it rolls over with the next reference clock cycle.

$$R = NP_A - \left(\left[\frac{NP_A}{W} \right]_{\text{truncated integer}} W \right) \tag{1}$$

Here R is the remaining number of points in the accumulator just before it rolls over. N is the number of cycles of the DDS output. P_A is the number of points in the phase accumulator. W is the frequency tuning word. The integer in square brackets is truncated not rounded. Fig. 5 depicts the transitions of the phase accumulator between the last point in the cycle and the next point in the new cycle. The image on the left shows the transition without a change in frequency. The image on the right shows the transition with a change in frequency.

The y-axis represents the phase point number. The x-axis is time. $\boldsymbol{\tau}_{RC}$ is the period of the reference clock. $\boldsymbol{\tau}_R$ is the time from the last point in the wave to the zero crossing. $\boldsymbol{\tau}_S$ is the time from the zero crossing to the next point. The number of points in the accumulator at the first reference clock cycle in the waveform after the zero crossing is defined as S without a frequency transition and as S' after a frequency transition. They are given by:

$$S = \frac{W\boldsymbol{\tau}_S}{(\boldsymbol{\tau}_S + \boldsymbol{\tau}_R)} \text{ and } S' = \frac{W'\boldsymbol{\tau}_S}{(\boldsymbol{\tau}_S + \boldsymbol{\tau}_R)} \tag{2}$$

respectively and

$$\boldsymbol{\tau}_R = \frac{R\boldsymbol{\tau}_{RC}}{W} \text{ and } \boldsymbol{\tau}_S = \boldsymbol{\tau}_{RC} - \boldsymbol{\tau}_R \tag{3}$$

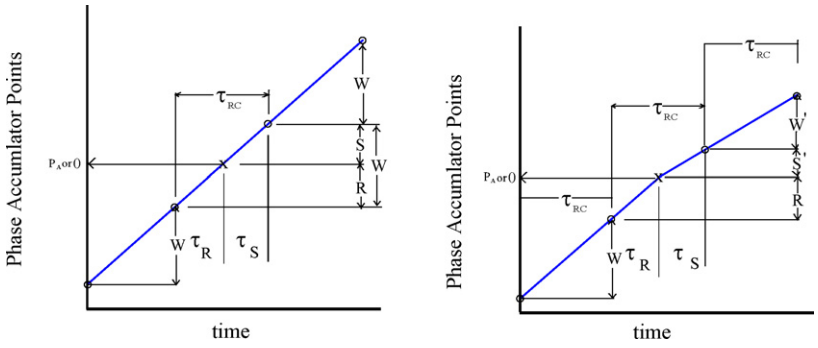

Fig. 5. A depiction of the transition of the phase accumulator between the last point in the cycle and the next point in the new cycle. On the left, the transition is depicted without a change in frequency. On the right, the transition is depicted with a change in frequency. The *X* marks the rollover point and the circles represent the value in the phase accumulator at each reference clock transition. *W* represents the change in the accumulator points at each reference clock transition and *W*′ represents the change at the new frequency.

Values that change at the frequency transition are indicated with a prime (′). Note that the phase shifts are defined so that the output waves of the two DDS chips are precisely an integer number of reference clock pulses apart. The phase shifts in radians of the first and second DDS are respectively, ϕ_1 and ϕ_2:

$$\phi_1 = \frac{2\pi}{P_A} S' \text{ and } \phi_2 = \frac{2\pi}{P_A}[P_A - R'] \quad (4)$$

The term, $(2\pi/P_A)$, results from the phase wheel being divided into P_A points. The quantity in brackets [ ] in the equation for ϕ_2 results from the number of points in the accumulator rolling over at the zero crossing. Then substituting (2) and (3) into (4) to obtain:

$$\phi_1 = 2\pi \left(\frac{W'}{P_A}\right)\left(\frac{\tau_S}{\tau_S+\tau_R}\right) \text{ and } \phi_2 = 2\pi\left[1 - \left(\frac{W'}{P_A}\right)\left(\frac{\tau_S}{\tau_S+\tau_R}\right)\right] \quad (5)$$

The phase-shifted value is defined as the angle formed by first *n* points of the phase wheel using new frequency starting at a phase angle of zero. The above equations can be generalized to the *i*th frequency change:

$$R_i = \left[N_i * P_A + W_i\left(\frac{\tau_{R(i-1)}}{\tau_{RC}}\right)\right] - \left(\left\{\frac{N_i * P_A + W_i((\tau_{R(i-1)})/(\tau_{RC}))}{W_{i+1}}\right\}_{\text{truncated integer}} * W_{i+1}\right) \quad (6)$$

$$\phi_1^{i-1} = 2\pi\left(\frac{W_i}{P_A}\right)\left(\frac{\tau_{R(i-1)}}{\tau_{S(i-1)}+\tau_{R(i-1)}}\right) \text{ and}$$

$$\phi_2^{i-1} = 2\pi\left[1 - \left(\frac{W_i}{P_A}\right)\left(\frac{\tau_{R(i-1)}}{\tau_{S(i-1)}+\tau_{R(i-1)}}\right)\right] \quad (7)$$

Finally, we can modify the solution to account for the lower resolution of the phase offset word. Current DDS technology puts the phase offset word resolution at up to 14 bits. We can generalize that to *m* bits as follows:

$$\phi_1^{i-1} = \frac{2\pi}{2^m}\left\{2^m\left(\frac{W_i}{P_A}\right)\left(\frac{\tau_{R(i-1)}}{\tau_{S(i-1)}+\tau_{R(i-1)}}\right)\right\}_{INT} \quad (8)$$

and

$$\phi_2^{i-1} = \frac{2\pi}{2^m}\left\{2^m\left[1 - \left(\frac{W_i}{P_A}\right)\left(\frac{\tau_{R(i-1)}}{\tau_{S(i-1)}+\tau_{R(i-1)}}\right)\right]\right\}_{INT} \quad (9)$$

Note that the phase shift may not have to be exactly equal to the angle. However, the error approaches zero if the phase shift is arbitrarily close to the angle but less than the exact value. Moreover, adding an adjustment to the phase differential can compensate for any additional measurable delays. The DAC output of second DDS is then filtered of all the high frequency components creating a smooth frequency transition that always occurs at the zero crossing point in the sine wave. In this case, the frequency transition is jitterless or phase coherent.

Our derivations show that the phase shifts can be precisely calculated for each frequency shift at any cycle of the output wave. Current field programmable gate array and embedded-processor technology can easily keep up with the DDS so that the waveforms and frequencies can be changed at MHz rates. Alternatively, one may use a very fast counter (possibly a very fast FPGA when it becomes available) to count the sample points necessary before the zero crossing occurs. Another alterative is to produce a chip with two accumulators and have one of the accumulators run an integer number of steps ahead of the other. In these cases, only one DDS is necessary.

Additionally, it is possible to use the directly synthesized square wave from the first DDS because the triggering of the frequency change happens on the cycle of the reference clock so that better temporal resolution is not needed. The second DDS output wave is the programmable clock of the arbitrary waveform generator. The frequency step resolution and reproducibility achievable with this DDS-based technology for the arbitrary waveform generation is phenomenal. The temporal resolution of the arbitrary wave is defined by the jitter or reproducibility of the individual adjustable clock cycle. Adding more clock cycles or increasing the adjustable clock frequency will increase the temporal resolution of the arbitrary wave.

For example, a square waveform produced with *N* clock cycles will have *N* times the temporal resolution of a single clock cycle. This resolution is extendable all the way down to the 1 Hz range or lower by adding more points to define the arbitrary waveform. Large frequency changes or jumps can also be jitterless by accessing separate waveforms in the programmable memory and the number of counts that define the wave. Our technology permits scanning or jumping the frequency while maintaining high resolution and jitterless transitions anywhere in the available frequency spectrum. This scanning capability is better than that currently available from the best 20 GHz waveform generators. Multiple DDS chips can be coupled together to synchronize their output. Pulses can be delivered with excellent delay resolution relative to each other. This technology has phenomenal implications for scientific measurements such as mass spectrometry and NMR, arbitrary waveform generation, timing and gating.

3. Integration of the FPGA with DDS

The derivations of the previous section allow the phase of the waveform to be predicted and adjusted at any given time. The only

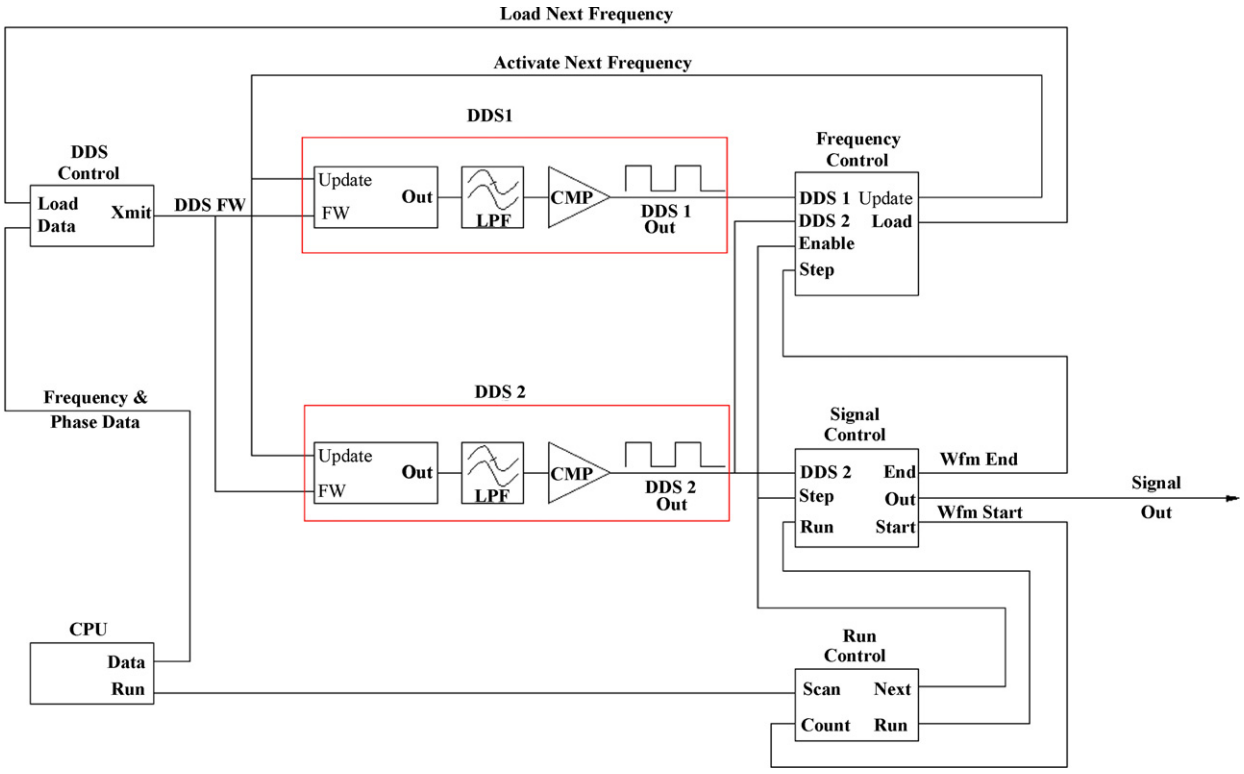

Fig. 6. Illustrates the interaction of the DDS devices with the programming blocks of the FPGA. The DDS devices are outlined in red rectangles. The rest of the black boxes represent blocks of the FPGA's programming that are used to control the stepping of the DDS and production of the waveforms applied to the trap during a mass scan.

elements needed to achieve phase-coherent frequency transitions is a device that can rapidly calculate and change the frequency tuning word and phase of the DDS and a method for triggering the update of the DDS device. In Fig. 6, we have depicted a block diagram of the program elements of the FPGA and their interaction with the DDS devices (outlined with red rectangles) to produce phase-coherent DDS frequency transitions. We did not include a schematic because most of the effort to produce phase-coherent frequency transitions from the DDS occurred within the FPGA; therefore, a schematic would not have been enlightening. The parameters of the mass scan were downloaded from a PC-based control programme developed in house to the central processing unit (CPU) block of the FPGA. The CPU block calculated the frequency and phase data used to operate the DDS devices. The frequencies of the trap waveforms were calculated from equations derived in a previous publication [7] so that the ejection mass-to-charge ratio could be stepped linearly under any scanning conditions. The frequencies were then used to calculate the frequency tuning word (FW) that defines the frequency of the DDS [10]. The CPU block then downloads the appropriate parameters corresponding to the desired DDS phase and frequency to each Control block via an internal data bus (not shown in the figure). The DDS Control block acts as a data buffer that transmits the 48-bit frequency and phase data (FW) to each DDS unit when commanded by the Frequency Control. The Run Control is the master timer that counts the number of cycles in the signal output and tells the Frequency Control to advance to the next frequency. The Run Control also enables the signal output of the Signal Control block. The Frequency Control block generates the frequency update signal and sends it to the DDS and also signals the DDS Control to send new frequency and phase data to the DDS.

Both DDS devices operate with the same frequency word; however, DDS 1 is phase shifted forward so that its output waveform period ends a fixed number of reference clock cycles before the output waveform period of DDS 2. The outputs of DDS 1 and 2 were entered into the Frequency Control block of the FPGA. The rising edge of the rectangular output of DDS 1 is used to trigger the update of the DDS data. The phase shift of DDS 1 relative to DDS 2 compensates for the DDS pipeline delay so that the update occurs at the clock cycle before the accumulator in DDS 2 rolls over. The phases of both DDS devices are shifted by the amounts calculated by Eqs. (8) and (9) and the new frequency word is applied. Eqs. (8) and (9) guarantee the temporal delay between the DDS devices remains at the specified number of clock cycles while the phase value in the accumulator of DDS 2 is shifted to its new projected value at the next clock cycle at the start of the new waveform. Note that the passage of the DDS digitized output through the low-pass filter (LPF) smoothes out the jitter caused by truncation and makes the period of the smoothed sine wave end at the correct point in time even when the frequency is shifted. The smoothed sine wave output is then passed through a comparator (CMP) that sets the output high when the amplitude of the sine wave is greater than zero and low when it is less than zero thereby producing a square wave output. The square wave output of DDS 2 entered the Signal Control block of the FPGA. The DDS 2 square wave output acted as the variable clock for the counters in the Signal Control block. These counters were used to create rectangular waveforms applied to the ion trap. The duty cycle (0–100%) and phase of the rectangular waveforms relative to the waveform start (Wfm Start) could be adjusted with input from the CPU.

4. Demonstration of the transition jitterless DDS frequency stepping

To demonstrate the concept of jitterless or phase-coherent DDS frequency stepping, a prototype waveform generator was built from four 300 MHz commercial DDS test boards (Analog Devices, AD9852) combined with a field programmable gate array with a 32-bit embedded-processor architecture (NIOS II) from Altera, Inc. Two DDS each were required to provide the waveforms for ring and end caps. The phase-coherent output of the DDS was digitally

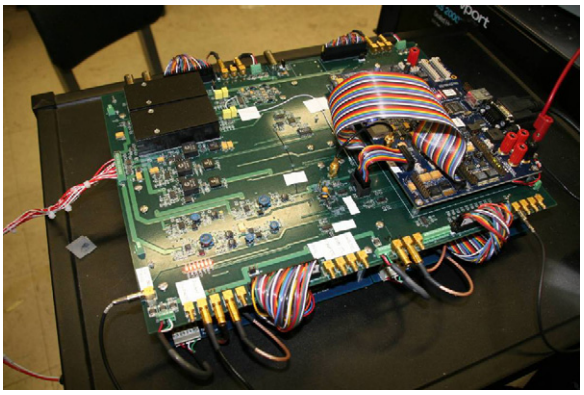

Fig. 7. An image of the prototype waveform generator. The prototype waveform generator was built from four 300 MHz commercial DDS test boards (Analog Devices, AD9852) combined with a field programmable gate array with a 32-bit embedded-processor architecture (NIOS II) from Altera, Inc. The phase-coherent output of the DDS was digitally processed on a separate board with counters to produce rectangular waveforms. The filtered DDS square wave TTL output had a jitter of 20 ps. Rectangular waveform generation using the TTL output to operate digital counters worked well but significantly increased the jitter. Resampling techniques were used to reduce the arbitrary square waveform jitter to approximately 100 ps.

processed on another board with counters to produce rectangular waveforms. This system for rectangular wave production was designed to operate a digital ion trap mass spectrometer [3], an application that requires rapid stepping of the waveform frequency to produce a viable mass spectrum. The prototype waveform generator is depicted in Fig. 7. Our prototype performed much better than expected considering it is the tiered integration of off-the-shelf test boards. The filtered DDS square wave TTL output had a jitter of 20 ps. Rectangular waveform generation using the TTL output to operate digital counters worked well but significantly increased the waveform jitter. Resampling techniques were used to reduce the arbitrary rectangular waveform jitter to approximately 100 ps.

The prototype delivered two separate phase-coherent rectangular waveforms. Their output was used to produce the waveforms for the ring and two endcap electrodes. The output for the ring electrode was amplified using a high voltage DC pulser from Directed Energy Inc. The pulser switched the voltage between ±750 V maximum. Care was taken to limit the output power of the pulser to less than 150 W by limiting the voltage as suggested by the manufacturer. The dipolar endcap voltages were generated directly from the prototype. A graphic user interface (GUI) was developed in house to operate and monitor the prototype. The frequency stepping was automatically adjusted using a mathematical expression for resonant ejection from a digital ion trap derived by our group [7] to yield a fixed mass increment for each frequency step. The GUI could be used to phase lock the endcap and ring TTL waveforms on-demand so that the endcap frequency was equal to the ring frequency divided by an integer. The top trace in the oscilloscope image (Fig. 8) shows the ring waveform transitioning between 100 and 50 kHz. The bottom trace in Fig. 8 shows the endcap waveform. In this case, the endcap output was phase locked to the ring output and was programmed with a 25% duty cycle. The endcap waveform was also phase shifted by 270°.

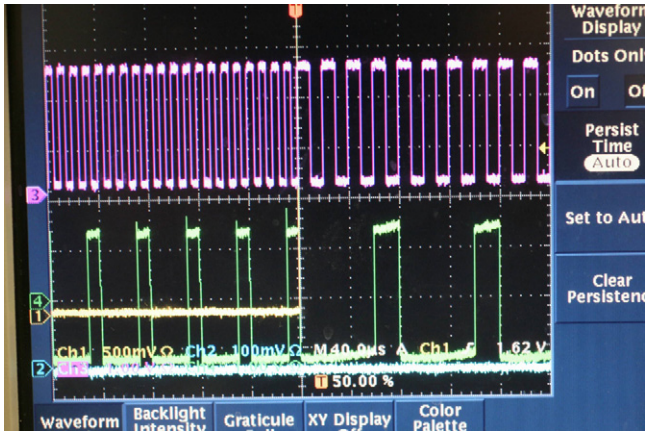

Fig. 8. The image of the waveform generator output displayed on an oscilloscope. The top trace depicts the ring waveform transitioning between 100 and 50 kHz. The bottom trace shows the endcap waveform. In this case, the endcap output was phase locked to the ring output and was programmed with a 270° phase shifted, 25% duty cycle. A separate pulse from the FPGA was used as a marker to identify the switching point and trigger the oscilloscope. With this marker, no discernable evidence of frequency transition jitter was observed. When the frequency of the ring waveform was switched or stepped, the frequency transition always occurred at the programmed time during the arbitrary waveform.

Due to the nature of the DDS device, frequency transitions are continuous in phase and not visible in the output. Therefore, a separate pulse from the FPGA was used as a marker to identify the switching point. With this marker, no discernable evidence of frequency transition jitter was observed. Without our phase-coherent technique the frequency transition jitter would have been as much as 10 μs (i.e., the period of the first waveform). Therefore the jitter would have been clearly visible in the oscilloscope trace. When the frequency of the ring waveform was switched or stepped, the frequency transition *always* occurs at the end of the cycle before the frequency switches during the production of the arbitrary waveform.

The multi-board architecture of the prototype waveform generator limited the rate of frequency change to roughly 1 MHz. This rate was more than sufficient for the ion trap mass spectrometer application that required frequency changes to occur after a minimum of four cycles of the ring waveform (<1 MHz). However, in DDS devices, a frequency change occurs when a new frequency tuning word is downloaded. Our DDS devices used 48-bit tuning words to define the frequency. Three 300 MHz system clock cycles (10 ns) were required to write the word and then the frequency change was executed after another 10 ns delay.

The prototype was demonstrated by using it to produce the waveforms to operate a digital ion trap mass spectrometer. We used it to measure the electron impact ionization spectrum of a standard mass calibrant, perfluorotributylamine (PFTBA). The digital ion trap mass spectrum is shown in Fig. 9. The mass resolution of the digital ion trap increased dramatically when resonance ejection was used. Resonant ejection was performed by applying an asymmetric square wave voltage on the end cap electrodes to produce dipolar excitation [13]. The mass spectrum shown in Fig. 9 was performed using the phase-unlocked mode [7] where the trapping frequency was scanned while endcap frequency was held constant at 100 kHz. The trapping potential voltage was 500 V_{p-p} and was stepped from approximately 350 to 280 kHz. The frequency was stepped nonlinearly according to the equation derived by our group [7] to yield a linear mass step of 0.005 Th. The frequency at each mass step was cycled 60 times to achieve a resolution of approximately 5000 ($m/\Delta m$) at a scan rate of 25 Th/s in approximately 6 s. Decreasing the number of cycles per mass step and the mass step size did not seem to change the resolution much. The effect of phase locking was not significant under our experimental conditions. Assuming that the resolution, $m/\Delta m = T/2\Delta T$, where T is the period of the arbitrary waveform, this mass resolution corresponds to a temporal resolution (ΔT) of about 275 ps. This number is greater than the measured 100 ps jitter of the generated waveforms. However, other factors such as DC voltage fluctuations and waveform overshoot also significantly affect mass resolution. Waveform overshoot should not contribute significantly to the resolution at this level because phase locking the trapping and excitation waveforms while adjusting the

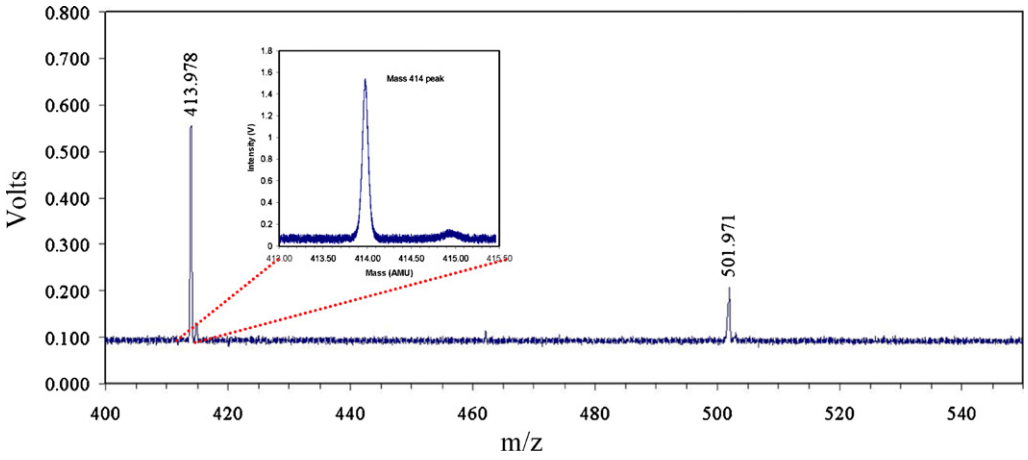

Fig. 9. An electron impact ionization digital ion trap mass spectrum of a standard mass calibrant, perfluorotributyl amine (PFTBA). Resonant ejection was performed in the phase-unlocked mode where the trapping frequency was scanned while the endcap frequency was held constant at 100 kHz. The resolution in the phase-unlocked mode achieved a mass resolution of approximately 5000 ($m/\Delta m$) at a scan rate of 25 Th/s (see the inset). The effect of phase locking was not significant under our experimental conditions. This mass resolution corresponds to a temporal resolution of about 275 ps assuming other factors such as DC voltage fluctuations and waveform overshoot to be insignificant. The resolution shown here was mainly limited by the temporal jitter associated with the waveform generation system and DC voltage fluctuations in the power supplies switched by the pulser.

duty cycle and delay of the excitation waveform did not noticeably improve the resolution [3]. The resolution exhibited in Fig. 9 was mainly limited by the voltage fluctuations in the DC power supplies that set the high and low limits of the rectangular high voltage waveform. These were switching power supplies that had approximately a 0.1% voltage ripple. Better power supplies should yield better resolution.

These factors can be markedly improved in future generations of the waveform production system. Presumably, the temporal jitter of the arbitrary waveform can be reduced to the jitter of the phase-coherent variable clock (~20 ps). Additionally, it is also reasonable to expect to reduce the DC power supply fluctuations to the part per million range with appropriate filtering techniques. Improving the resolution by an order of magnitude or more at m/z 414 should feasible. We also point out that the limiting factors of clock jitter, DC fluctuations and waveform overshoot become less important in a higher mass range where the period of the driving waveform is longer because they do not change as a function of waveform period. Consequently, the mass resolution should improve as the square root of the mass because the mass is proportional to the square of the period. The ring voltage can also be increased at lower frequencies because heat dissipation within the MOSFET-based pulser is less of an issue.

5. Impact of phase-coherent clock frequency transitions in arbitrary wave production

Theoretically, frequency changes can be accomplished at 100 MHz rates with a 300 MHz 48-bit DDS device. The period of the clock waveforms that can be generated has essentially a continuous range of values with the increments being infinitesimal relative to the jitter. For example in our device, the temporal increment of a 10 MHz DDS generated waveform upon incrementing the tuning word by one unit would change the period of the wave by 10^{-20} s. Obviously a 10^{-20} s change in the period is not meaningful because the waveform jitter is 20 ps (~2×10^{-11} s). However, this shows that the change in the period of the waveform is essentially continuous and precise. The maximum frequency of the DDS is the Nyquist frequency (1/2 the internal clock frequency), theoretically. Practically, the maximum is about 0.4 times the internal clock frequency [10]. For a 300 MHz device that would be 120 MHz maximum. The minimum time between points in the arbitrary wave is then 8.3 ns, but the spacing between the points in the arbitrary waveform can be rapidly changed ($\leq$ 100 MHz) from one point to the next with an essentially continuous and precise range of values. With this generator method, the frequency of the DDS output could be changed after each output cycle assuming the output frequency stayed below 100 MHz; if not, it would be once every two cycles. Transitions in the output waveform do not have to be spaced by an integer number of clock cycles at a single frequency as in the current state of the art. Consequently, even complex waveforms with multiple unevenly spaced transitions can be generated without error [10].

The application that led to our developing this technology was digital ion trap mass spectrometry [3]. In digital ion trap and quadrupole mass spectrometry, the control of the square wave duty cycle and rapid stepping of the frequency is important [8]. When we began developing our digital ion trap, no commercial waveform generator existed that could generate and change the waveforms with enough rapidity and precision to be viable. Our waveform generation technique provides these requirements with excellent resolution and accuracy. Rectangular waveforms of this type could easily be generated in a frequency shift keying (FSK) operation where the duration of the high in the output wave is precisely defined by an integer number of clock pulses at frequency 1 and the low duration is defined by another integer number of clock pulses at frequency 2. Frequencies 1 and 2 can then be stepped to change the frequency and/or duty cycle of the rectangular waveform. This simplistic method yields precise control of the ions in the trap and can be used for exact ion isolation, collision-induced dissociation and high resolution analysis. With our technology, the control over the duty cycle is also 48 bit, instead of a maximum of 16 bit with normal DDS operation. Our results suggest that a jitter-based resolution of 20 ps or less could be achieved assuming the waveform generator limits the resolution. Consequently, if other sources of resolution loss, such as DC fluctuations and waveform overshoot, are carefully controlled, much better mass resolution than the 19,000 at m/z 1500 with a 50 ps step resolution of the waveform period and their maximum jitter of 500 ps observed by Ding et al. [3] should be achievable.

For the prototype, we used counters to create the rectangular waves for simplicity and because of the multi-board structure. Using counters introduced large amounts of jitter; however there are commercial DACs available that could easily be used with our DDS-based clock system to generate the waveforms with more versatility and much lower jitter than produced by our prototype.

Ideally, the DACs, DDS and FPGA would be integrated on a single board to minimize delays. The proposed method could then be used to generate the digital ion trap waveforms with phenomenal agility, precision and accuracy. It is the precision and frequency-stepping resolution of the applied waveforms that ultimately defines the capabilities of digital ion traps. Our work has demonstrated a methodology that can be used to greatly increase the precision of the applied waveforms and provide phenomenal control of the duty cycle and the relative phase. These abilities will increase the resolution and MS/MS capabilities of digitally-driven ion traps and quadrupoles. Our work represents a significant step in bringing digital ion traps into the mainstream.

6. Conclusions

A method for triggering DDS devices to change frequency with phase coherence has been conceived and developed. The technique was demonstrated by developing a waveform generator to operate a digital ion trap mass spectrometer. The prototype digital ion trap waveform generator performed well yielding a resolution of 5000 ($m/\Delta m$) at $m/z = 414$. Further development of the waveform generation system is expected to yield significantly better resolution—as much as an order of magnitude at m/z 414 should be achievable. Better resolution is expected at higher mass-to-charge ratios with the resolution increasing as the square root of mass.

The development of the phase-coherent variable clock permits precise timing and the rapid changing of the timing of events during the production of arbitrary waves. This advance fundamentally increases the complexity, resolution and precision with which arbitrary waveforms can be produced. It is our contention that the ramifications of the ability to produce much more temporally complex waveforms will be subtle yet its effect could eventually be transformational because we have added a second variable, time, to the production of arbitrary waveforms.

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